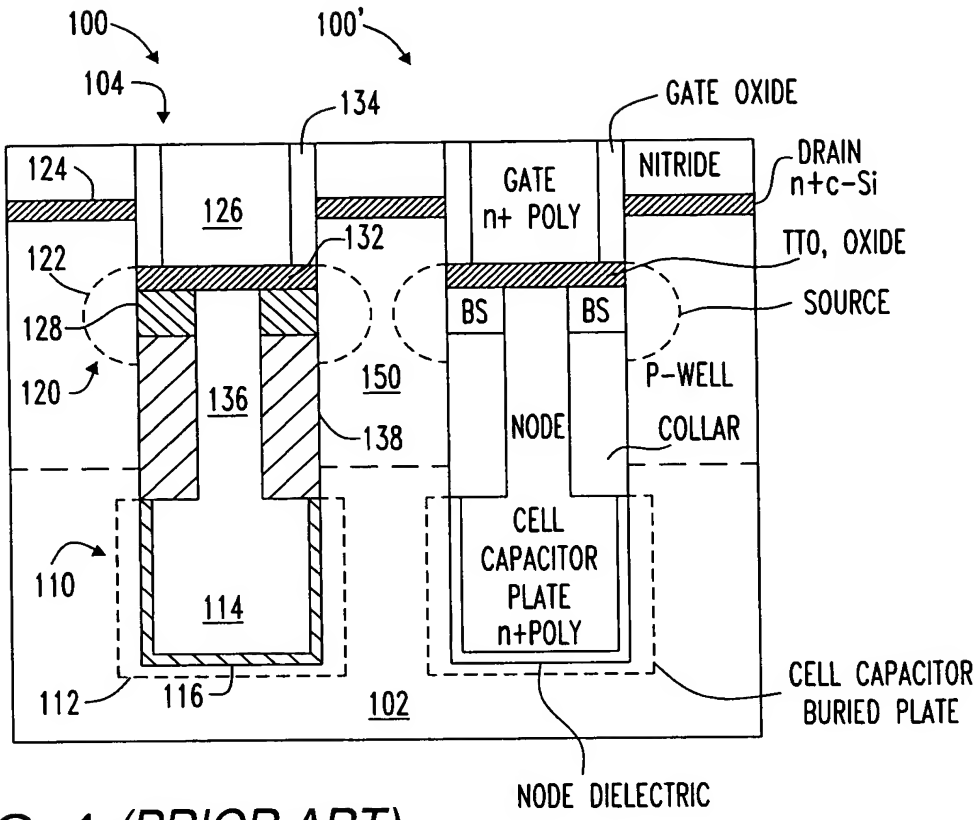

FIG. 1 *(PRIOR ART)*

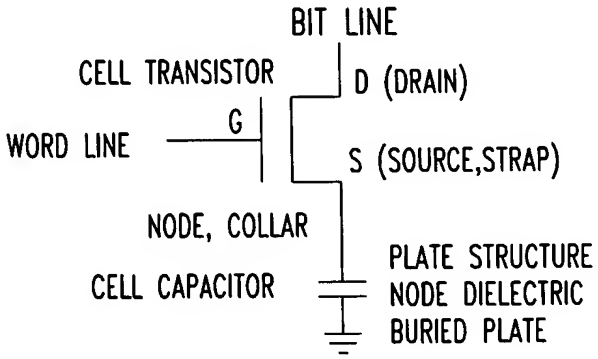

FIG. 1A *(PRIOR ART)*

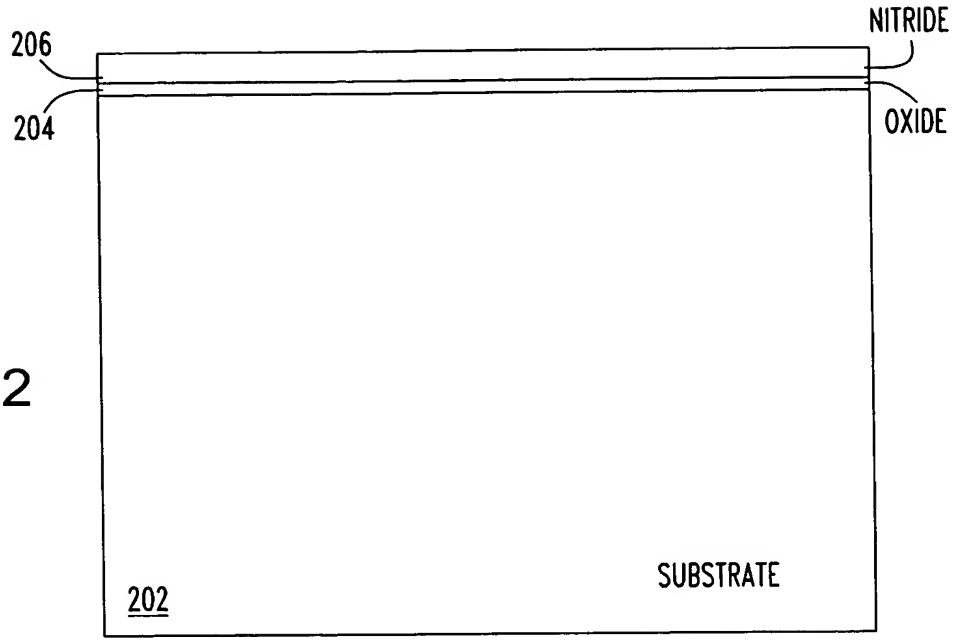
206
204
NITRIDE
OXIDE
SUBSTRATE
202

FIG. 2

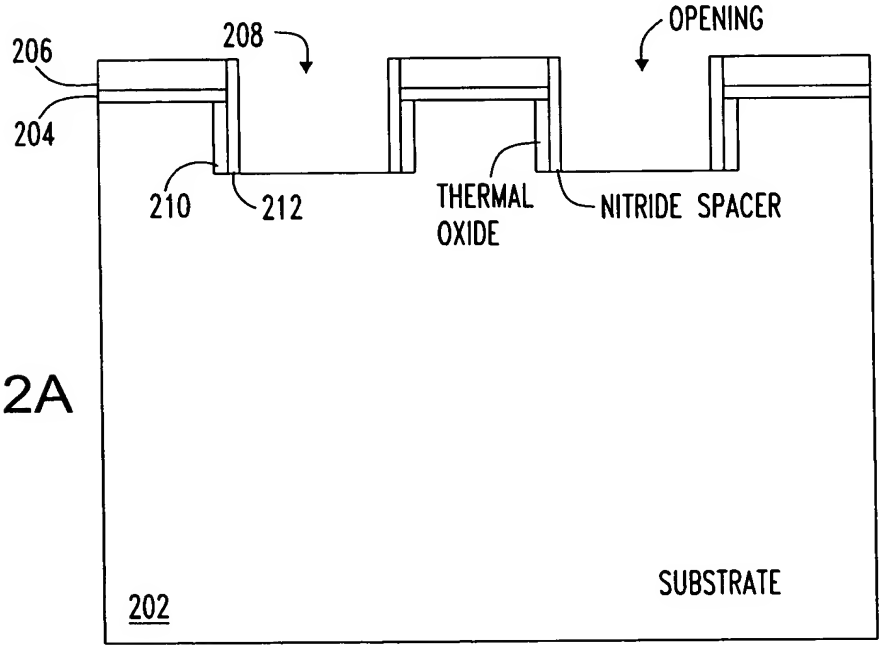
206
208
OPENING
204
210
212
THERMAL
OXIDE
NITRIDE SPACER
SUBSTRATE
202

FIG. 2A

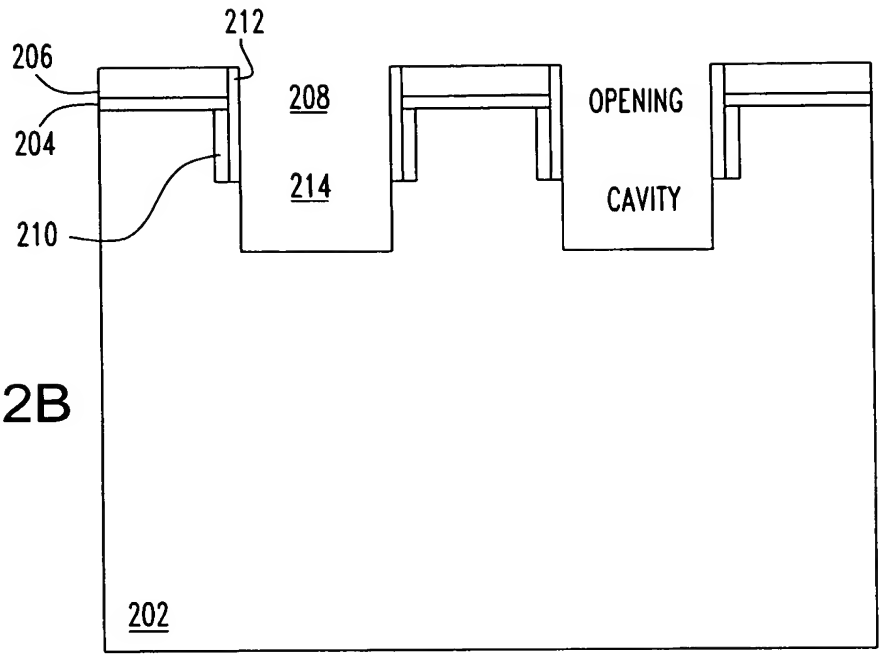
212
206
208
OPENING
204
214
CAVITY
210
202

FIG. 2B

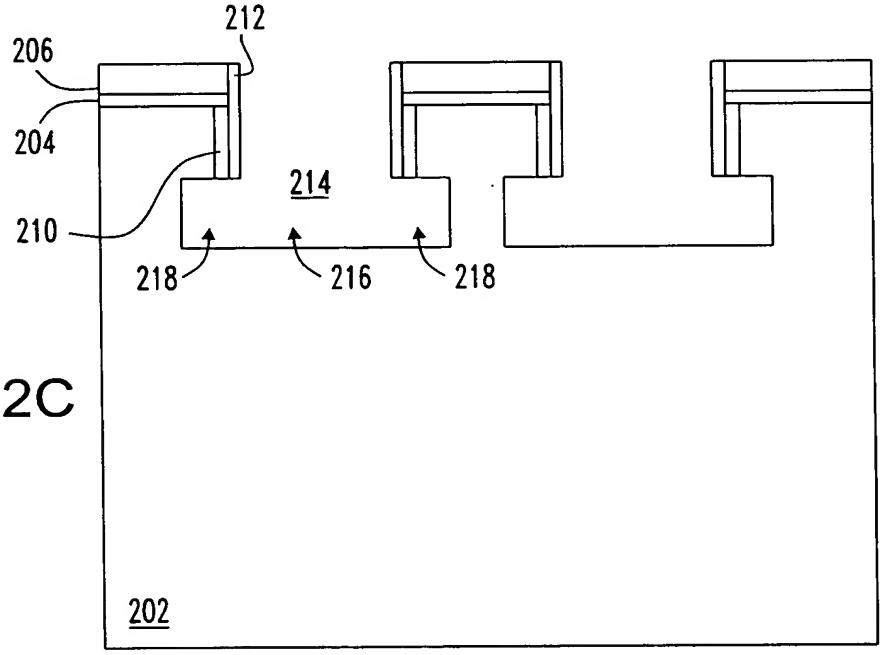
212
206
204
214
210
218
216
218
202

FIG. 2C

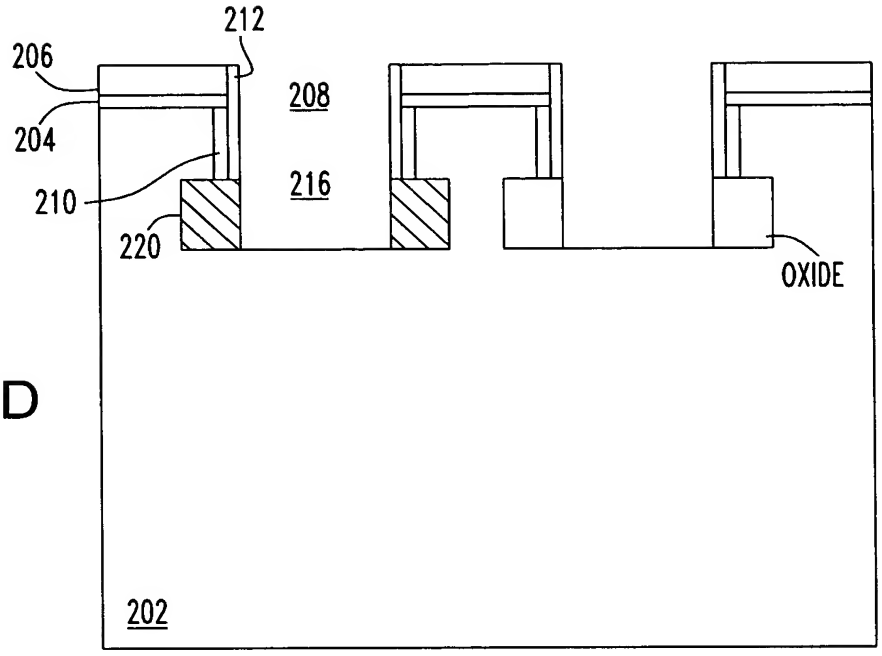
212
206
208
204
216
210
220
OXIDE
202

FIG. 2D

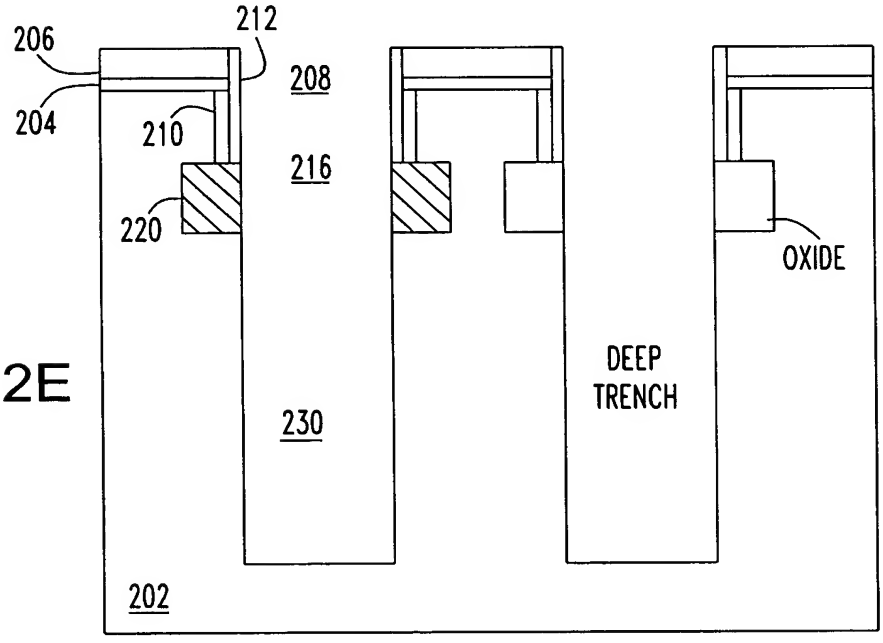
212
206
208
204
210
216
220
OXIDE
DEEP
TRENCH
230
202

FIG. 2E

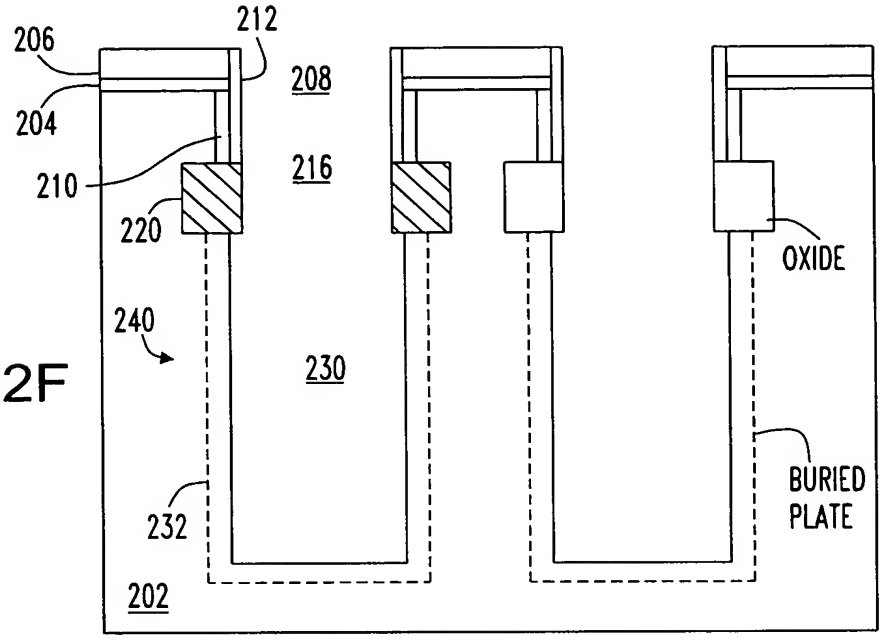
206
212
208
204
216
210
220
OXIDE
240
230
BURIED
PLATE
232
202

FIG. 2F

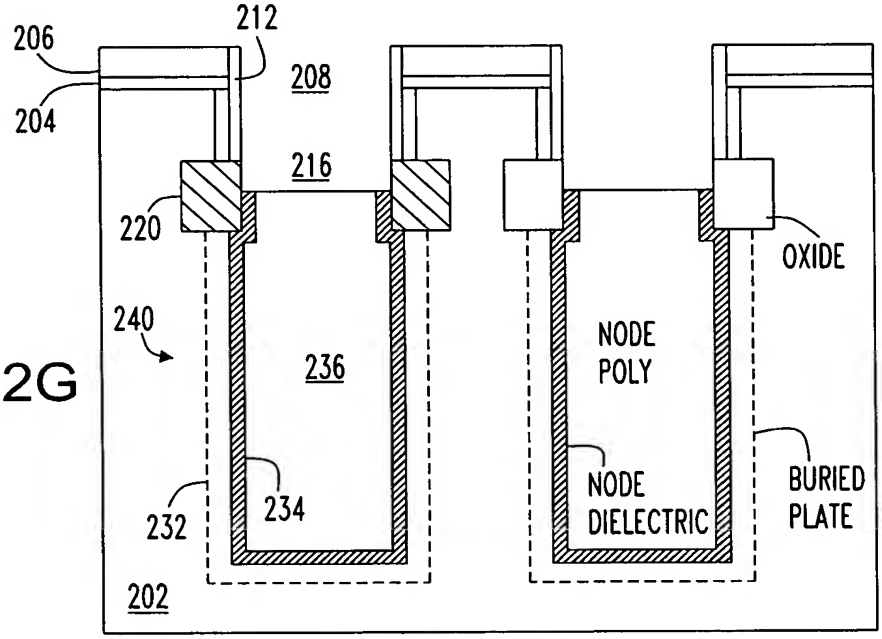
206
212
208
204
216
220
OXIDE
240
NODE
POLY
236
234
NODE
DIELECTRIC
BURIED
PLATE
232
202

FIG. 2G

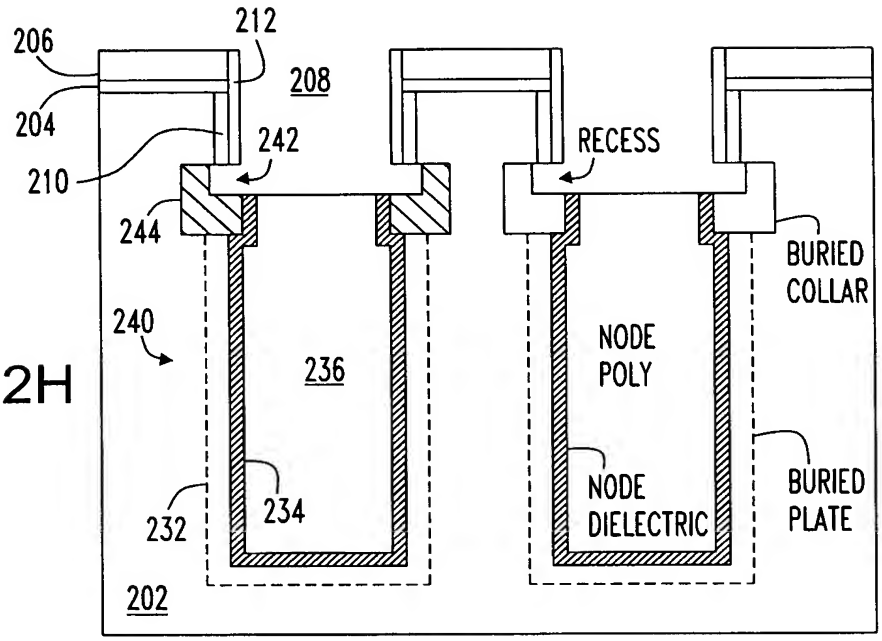
206
212
208
204
242
RECESS
210
244
BURIED
COLLAR
240
236
NODE
POLY
NODE
DIELECTRIC
BURIED
PLATE
232
234
202

FIG. 2H

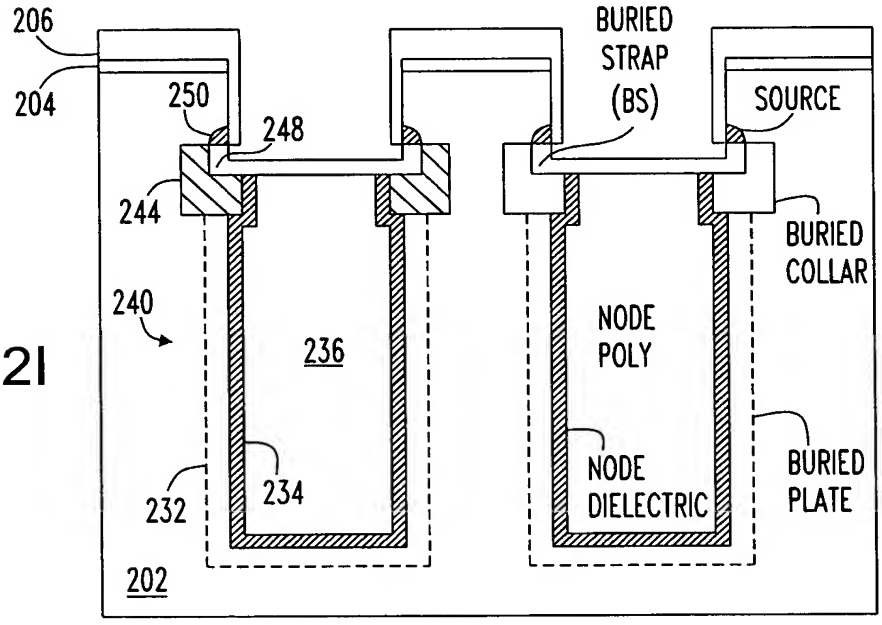
206
204
250
248
BURIED
STRAP
(BS)
SOURCE
244
BURIED
COLLAR
240
236
NODE
POLY
NODE
DIELECTRIC
BURIED
PLATE
232
234
202

FIG. 2I

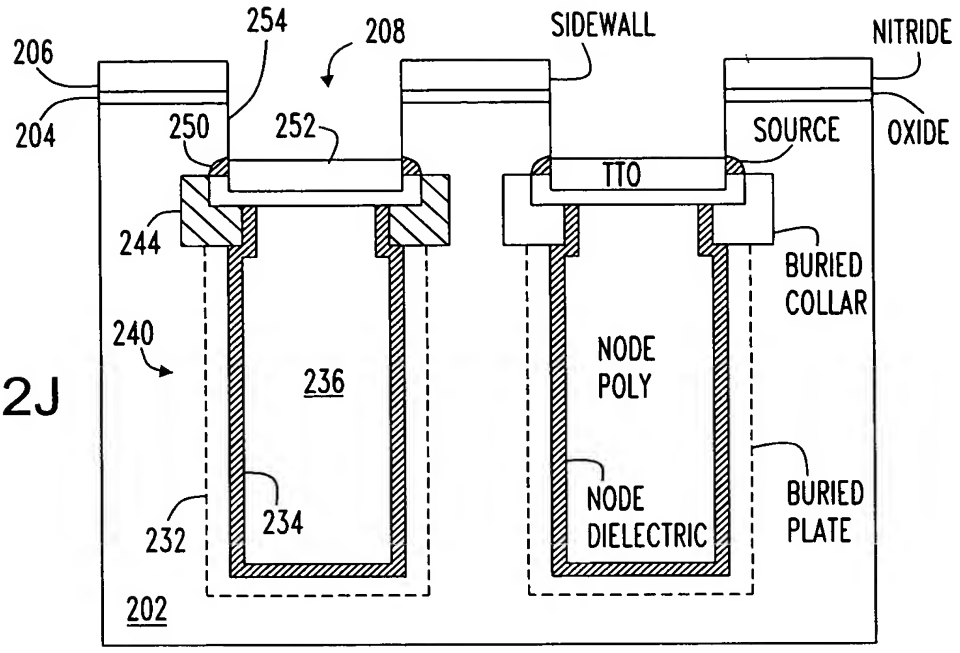
206
204
254
208
SIDEWALL
NITRIDE
250
252
SOURCE
OXIDE
TTO
244
BURIED
COLLAR
240
236
NODE
POLY
NODE
DIELECTRIC
BURIED
PLATE
232
234
202

FIG. 2J

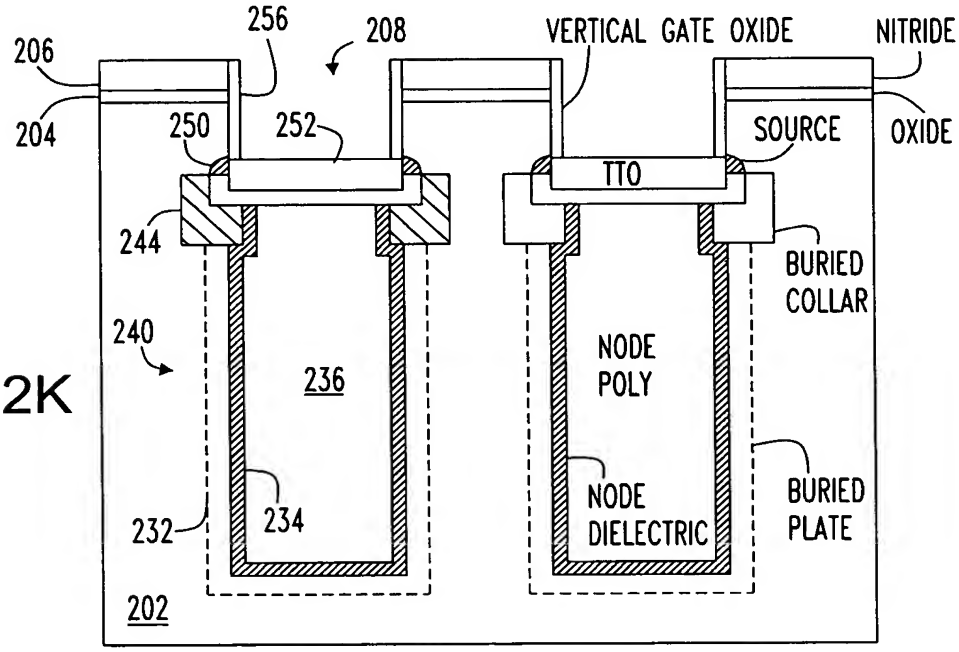
206
204
256
208
VERTICAL GATE OXIDE
NITRIDE
250
252
SOURCE
OXIDE
TTO
244
BURIED
COLLAR
240
236
NODE
POLY
NODE
DIELECTRIC
BURIED
PLATE
232
234
202

FIG. 2K

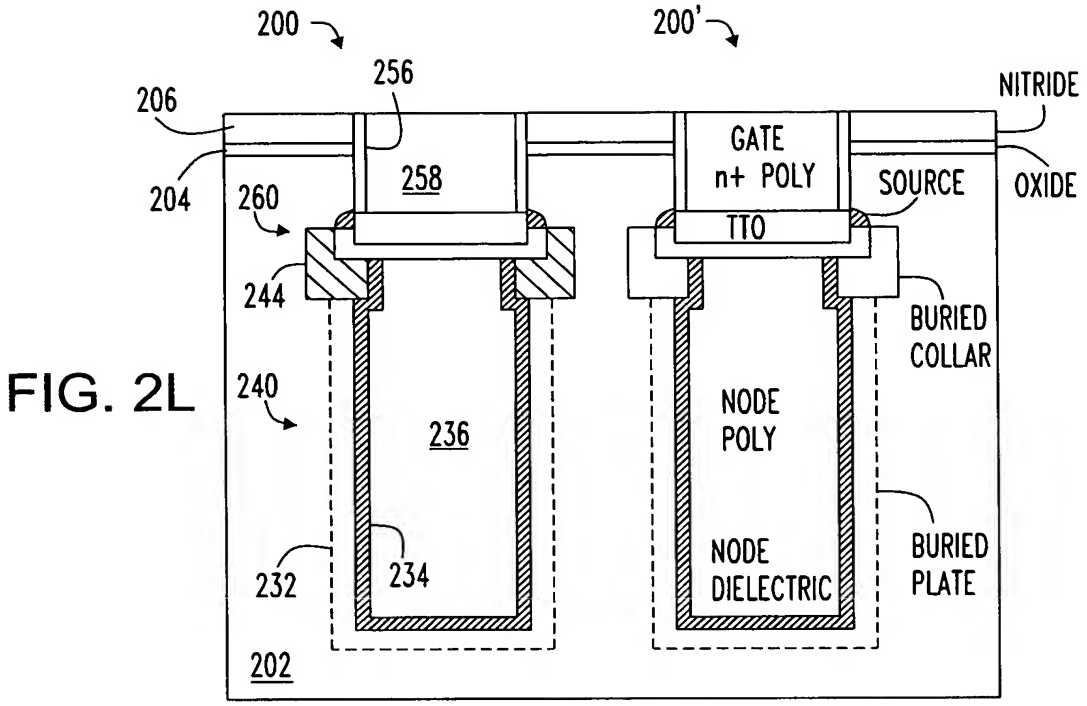
200
200'
256
206
NITRIDE
GATE
n+ POLY
SOURCE
OXIDE
204
258
260
TTO
244
BURIED
COLLAR
240
236
NODE
POLY
NODE
DIELECTRIC
BURIED
PLATE
232
234
202

FIG. 2L

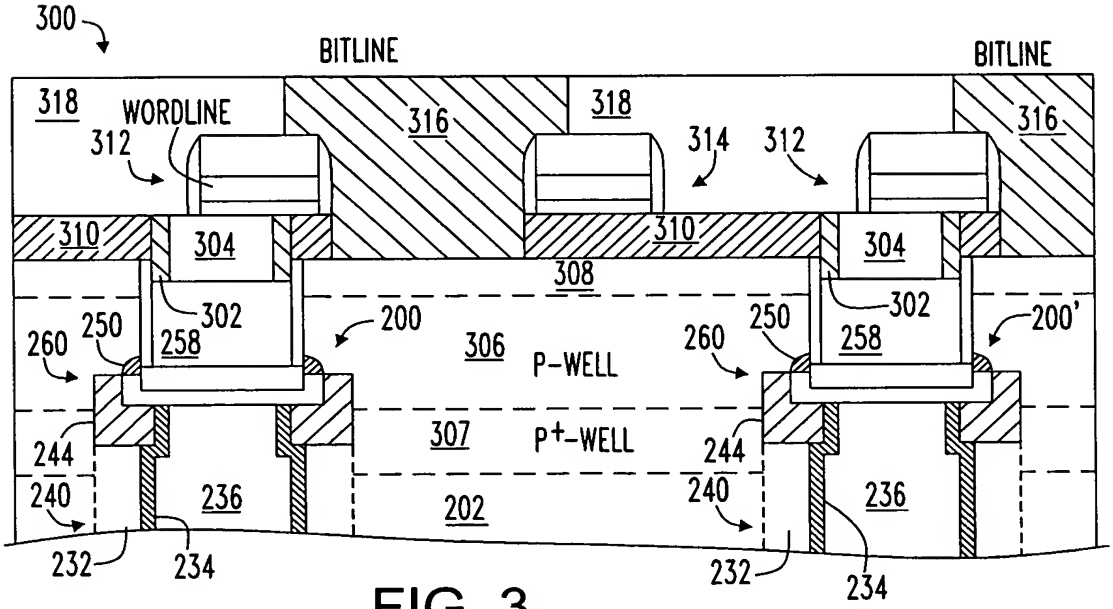
300
BITLINE
BITLINE
318
WORDLINE
316
318
316
312
314
312
310
304
310
304
308
302
302
200
250
250
200'
260
258
306
P-WELL
260
258
307
P+-WELL
244
244
240
236
202
240
236
232
234
232
234

FIG. 3